CLAIMS

1. A network monitor that taps data from a network link between two network devices, the network monitor comprising:

first and second interfaces that allow the network monitor to be connected in-line in a network link between two network devices and to receive serial data therefrom and to transmit serial data thereto, each interface providing for serial-to-parallel conversion of data such that serial data received from a said network link at the interface is output as parallel data, and each interface providing for parallel-to-serial conversion of data such that parallel data received at the interface is output as serial data for transmission to a said network link; and,

first and second programmable logic devices,

the first programmable logic device being arranged to receive parallel data output by the first interface and to process said data for network analysis purposes, the second programmable logic device being arranged to receive parallel data output by the second interface and to process said data for network analysis purposes, each programmable logic device being controllable so as to selectively pass a copy of the received parallel data to the other programmable logic device so that the network monitor can operate in in-line mode and not to pass a copy of the received parallel data to the other programmable logic device so that the network monitor can operate in end station mode,

the second programmable logic device being arranged to pass the copy of the parallel data received from the first programmable logic device to the second interface for parallel-to-serial conversion and for transmission of the

serial data back to a said network link when the network monitor is operating in in-line mode,

the first programmable logic device being arranged to pass the copy of the parallel data received from the second programmable logic device to the first interface for parallel-to-serial conversion and for transmission of the serial data back to a said network link when the network monitor is operating in in-line mode.

2. A network monitor according to claim 1, comprising:

a first parallel data frequency and width adjuster between the first interface and the first programmable logic device, the first parallel data frequency and width adjuster being constructed and arranged to reduce the frequency and to increase the width of parallel data received from the first interface by a predetermined amount prior to said data being passed to the first programmable logic device; and,

a second parallel data frequency and width adjuster between the second programmable logic device and the second interface, the second parallel data frequency and width adjuster being constructed and arranged to increase the frequency and to reduce the width of parallel data received from the second programmable logic device by said predetermined amount prior to said data being transmitted to a said network link by the second interface when the network monitor is operating in in-line mode.

3. A network monitor according to claim 2, wherein the first parallel data frequency and width adjuster is provided by a multiplexer and the second parallel data frequency and width adjuster is provided by a demultiplexer.

4. A network monitor according to claim 2 or claim 3, comprising:

a third parallel data frequency and width adjuster between the second interface and the second programmable logic device, the third parallel data frequency and width adjuster being constructed and arranged to reduce the frequency and to increase the width of parallel data received from the second interface by a predetermined amount prior to said data being passed to the second programmable logic device; and,

a fourth parallel data frequency and width adjuster between the first programmable logic device and the first interface, the fourth parallel data frequency and width adjuster being constructed and arranged to increase the frequency and to reduce the width of parallel data received from the first programmable logic device by said predetermined amount prior to said data being transmitted to a said network link by the first interface when the network monitor is operating in in-line mode.

5. A network monitor according to claim 4, wherein the third parallel data frequency and width adjuster is provided by a multiplexer and the fourth parallel data frequency and width adjuster is provided by a demultiplexer.

6. A network monitor according to any of claims 1 to 5, comprising a clock signal provider for providing a clock signal so that data can be clocked through the network monitor.

7. A network monitor according to claim 6, wherein the clock signal provider is constructed and arranged to obtain said clock signal by recovering a clock signal from data received at the first and second interfaces respectively.

8. A network monitor according to any of claims 1 to 7, wherein each programmable logic device is a field programmable gate array.

9. A method of monitoring data on a network link, the method comprising:

receiving data in serial form from a network link;

converting the data in serial form to data in parallel form;

passing the parallel data to a first programmable logic device for processing for network analysis purposes;

controlling the first programmable logic device such that the method takes place selectively in in-line mode or in end station mode,

whereby in in-line mode the first programmable logic device provides a copy of the received parallel data, the copy of the received parallel data being converted to data in serial form, said serial data being transmitted back onto the network link, and

whereby in end station mode the first programmable logic device does not provide a copy of the received parallel data for conversion into serial form and transmission back onto the network link.

10. A method according to claim 9, comprising:

after converting the data in serial form to data in parallel form, reducing the frequency and increasing the width of the parallel data by a predetermined amount prior

to said parallel data being passed to the first programmable logic device; and,

when operating in in-line mode, increasing the frequency and reducing the width of the copy of the parallel data by the predetermined amount prior to the copy of the parallel data being converted to data in serial form for transmission back onto the network link.

11. A method according to claim 9 or claim 10, comprising recovering a clock signal from the data received in serial form from the network link and using the recovered clock signal when operating in in-line mode to clock the data throughout the step of converting of the data in serial form to the data in parallel form to the step of transmitting serial data being back onto the network link.